CLAIMS

Amend the claims as follows.

1. (Canceled)

2. (Currently amended) In a wireless receiver where a radio frequency signal is received, downconverted, and processed into in-phase (I) and quadrature (Q) signal paths, a method of automatic gain control (AGC) comprising:

(a) at a specified stage in an I/Q baseband strip containing multiple automatic gain control (AGC) stages, each of the AGC stages having locally generated control signals associated therewith:

detecting respective I and Q output signals received from respective I and Q variable gain amplifiers (VGAs) associated with the specified AGC stage to produce a detected I and Q signal, the detecting comprising~~:~~:

passing the respective I and Q output signals through respective high pass filters (HPFs) to remove direct current offsets,

rectifying each of the respective I and Q filtered output signals,

adding the respective I and Q rectified filtered output signals in an operational amplifier, and

passing the added I and Q rectified filtered output signal through a low pass filter (LPF) to produce the detected I and Q signal;

~~digitizing the detected I and Q signal to generate a digitized I and Q signal; and~~

~~adjusting with the associated control signal the respective I and Q VGAs for differences between the detected I and Q signal and a reference signal;~~

generating at least one digital counter signal responsive to the differences between the detected I and Q signal and at least one reference signal;

generating a control signal by multiplexing the at least one digital counter signal with the reference signal; and

controlling the respective I and Q VGAs with the control signal; and

(b) repeating (a) through each AGC stage~~; and~~

~~where the digitizing comprises~~

~~receiving in an analog to digital converter (ADC) the detected I and Q signal,~~

~~comparing the detected I and Q signal to the a reference signal, and~~

~~generating digital up/down and count/hold control signals~~.

3. (Canceled)

4. (Currently amended) The method of claim 2 ~~where the comparing comprises~~ comprising using a multi-level comparator and a logic circuit to generate the digital up/down and count/hold control signals.

5. (Currently amended) The method of claim 4 where the at least one digital counter signal includes at least digital up/down and count/hold control signals and where generating the at least one digital counter signal ~~adjusting~~ comprises:

receiving in an up/down counter the digital up/down and count/hold control signals; and

setting the gains of the respective I and Q VGAs.

6. (Previously presented) The method of claim 5 where the setting comprises:

if the detected I and Q signal falls outside a predefined boundary, modifying the gains of the respective I and Q VGAs until the respective I and Q output signals achieve desired magnitudes;

else, maintaining the gains of the respective I and Q VGAs.

7. (Previously presented) The method of claim 6 where the modifying comprises adjusting the respective I and Q VGAs at a fast rate if the detected I and Q signal is beyond a first predefined range or at a slow rate if the detected I and Q signal is beyond a second predefined range but not beyond the first predefined range.

8. (Previously presented) The method of claim 6 where the modifying comprises adjusting the respective I and Q VGAs at a large magnitude if the detected I and Q signal is

beyond a first predefined range or at a small magnitude if the detected I and Q signal is beyond a second predefined range but not beyond the first predefined range.

9. (Canceled)

10. (Currently amended) In a wireless receiver where a radio frequency signal is received, downconverted, and processed into in-phase (I) and quadrature (Q) signal paths, an automatic gain control (AGC) circuit comprising multiple AGC stages where each of the AGC stages includes:

(a) respective I and Q variable gain amplifiers (VGAs);

(b) a detector to detect respective I and Q output signals received from the respective I and Q VGAs and to produce a detected I and Q output signal;

(c) an analog to digital converter (ADC) to convert the detected I and Q output signal to a digital detected I and Q output signal;

(d) a digital engine to digitally adjust the respective I and Q VGAs ~~for differences between the detected I and Q output signal and a reference signal~~ responsive to the digital detected I and Q output signal;

where the detector comprises:

i. respective I and Q high pass filters (HPFs) to remove direct current (DC) offsets from the respective I and Q output signals;

ii. respective rectifiers communicating with the respective I and Q HPFs to change the respective filtered I and Q output signals from alternating current (AC) to direct current (DC);

iii. an operational amplifier (Op-amp) communicating with the rectifiers to add the rectified filtered I and Q output signals; and

iv. a low pass filter (LPF) communicating with the Op-amp to filter the added rectified filtered I and Q output signal to produce the detected I and Q output signal; and

where the ADC comprises:

i. a multi-level comparator to compare the detected I and Q output signal to at least one reference signal; and

ii. a logic circuit to generate at least one digital counter signal responsive to the multi-level comparator; and

where the digital engine comprises:

i. an up/down counter to generate an up/down counter signal responsive to the at least one digital counter signal; and

ii. a multiplexer to generate a control signal that digitally adjusts the respective I and Q VGAs by multiplexing the up/down counter signal with the at least one reference signal.

11. (Canceled)

12. (Previously presented) The automatic gain control circuit of claim 10 where the number of levels in the multi-level comparator is at least four.

13. (Currently amended) The automatic gain control circuit of claim 12 where the ~~digital engine comprises an~~ up/down counter ~~for setting~~ is adapted to set gains associated with the respective I and Q VGAs.

14.-19. (Canceled)

20. (Currently amended) A wireless receiver including a plurality of serially connected automatic gain control stages, each stage comprising:

I and Q variable gain amplifiers (VGAs) to generate I and Q signals, respectively;

a detector to generate a detect signal from the I and Q signals;

an analog to digital converter (ADC) to convert the detect signal to a digital detect signal;

digital engine to generate a control signal responsive to the digital detect signal and a reference signal;

~~where the ADC is enabled to~~

~~compare the detect signal to the reference signal, and~~

~~generate digital up/down and count/hold control signals as the digital detect signal; and~~

~~where the I and Q VGAs operate responsive to the control signal~~

where the detector comprises:

i. respective I and Q high pass filters (HPFs) to remove direct current (DC) offsets from the I and Q signals;

ii. respective rectifiers communicating with the respective I and Q HPFs to change the filtered I and Q signals from alternating current (AC) to direct current (DC);

iii. an operational amplifier (op amp) communicating with the rectifiers to add the rectified filtered I and Q signals; and

iv. a low pass filter (LPF) communicating with the op-amp to filter the added rectified filtered I and Q signal to produce the detect I and Q output signal; and

where the ADC comprises:

i. a multi-level comparator to compare the detect I and Q signal to at least one reference signal; and

ii. a logic circuit to generate at least one digital counter signal responsive to the multi-level comparator; and

where the digital engine comprises:

i. an up/down counter to generate an up/down counter signal responsive to the at least one digital counter signal; and

ii. a multiplexer to generate a control signal that digitally adjusts the I and Q VGAs by multiplexing the up/down counter signal with the at least one reference signal.

21. (Previously presented) The wireless receiver of claim 20 comprising:

I and Q buffer amplifiers between the variable gain amplifiers and the detector to buffer the I and Q signals, respectively.

22. (Currently amended) The wireless receiver of claim 20 where the ~~detector includes:~~ respective I and Q high pass filters are configured to generate I and Q filtered signals by removing direct current offsets from the I and Q signals.

23. (Currently amended) The wireless receiver of claim 22 where the ~~detector includes:~~ respective rectifiers communicating with the respective I and Q high pass filters are configured to change each of the I and Q filtered signals from alternating current to direct current, producing the I and Q rectified filtered signals.

24.-25. (Canceled)

26. (Currently amended) A method comprising~~:~~:

at each of a plurality of serially connected automatic gain control stages, each of the stages having a respective I variable gain amplifier with a respective I output signal and a respective Q variable gain amplifier with a respective Q output signal, generating a respective detect signal from the respective I and Q output signals;

at each of the stages, converting the respective detect signal to a respective digital detect signal;

at each of the stages, generating a respective control signal to control the respective I and Q variable gain amplifiers responsive to the respective digital detect signal;

at each of the stages, adjusting the respective I and Q variable gain amplifiers responsive to the respective control signal; and

where the generating comprises:

high pass filtering the I and Q output signals by removing direct current offsets from the respective I and Q output signals;

rectifying the high pass filtered I and Q output signals to thereby change the high pass filtered I and Q output signals from alternating current to direct current I and Q rectified signals;

summing the direct current I and Q rectified signals to generate summed I and Q output signals; and

low pass filtering the summed I and Q output signals to generate the detect signal; where the converting comprises:

comparing the ~~respective~~ detect signal to at least one respective reference signal via a multi-level comparator; and

logically manipulating the compared signal to generate at least one digital counter signals ~~a logic circuit~~; and

where the generating comprises:

logically manipulating the compared signal to thereby generate an up/down counter signal; and

multiplexing the up/down counter signal with the at least one respective reference signal to generate the control signal.

27.-33. (Canceled)